## AMENDMENTS TO THE CLAIMS

Please accept new Claim 19 as follows:

1. (Previously Presented) A delay-locked loop for receiving an external clock signal and synchronizing a phase of a feedback clock signal with a phase of the external clock signal, the delay-locked loop comprising:

a phase detector for comparing the phase of the external clock signal with the phase of the feedback clock signal and outputting a phase difference as an error control signal;

a delay line, comprising a plurality of delay cells having various unit time delays, for receiving the external clock signal, controlling the phase of the external clock signal to obtain an output clock signal and outputting the output clock signal, wherein the number of delay cells in operation is adjusted in response to a shift signal, wherein each delay cell is a differential amplifier having a resistor connected to a power supply voltage, wherein the resistor of each delay cell has a different resistance, to vary the unit time delay; and

a filter unit for generating the shift signal for selecting the number of delay cells in operation in the delay line, in response to the error control signal.

2. (Original) The delay-locked loop of claim 1, wherein the delay line is structured such that a unit time delay gradually increases from the delay cell of a front end of the delay line to the delay cell of a rear end of the delay line.

3. (Cancelled)

4. (Previously Presented) The delay-locked loop of claim 1, wherein the resistance is gradually increased from the delay cell of a front end of the delay line to the delay cell of a rear end of the delay line.

5-13. (Cancelled)

14. (Previously Presented) A time delay compensation circuit for synchronizes an output clock signal with an external clock signal, the time delay compensation circuit comprising:

a delay unit, comprising a plurality of delay cells having various unit time delays, for receiving the external clock signal and generating the output clock signal in synchronization with the external clock signal, wherein each delay cell is a differential amplifier having a resistor connected to a power supply voltage, wherein the resistor of each delay cell has a different resistance, to vary the unit time delay; and

a control unit for selecting a number of delay cells in the delay unit and controlling the number of delay cells in operation such that the output clock signal is synchronized with the external clock signal.

15. (Original) The circuit of claim 14, wherein the delay cells of the delay unit have gradually increasing unit time delays from the delay cell at the front end of the delay unit to the delay cell at the rear end of the delay unit.

16-17. (Cancelled)

18. (Previously Presented) The circuit of claim 14, wherein the resistance is gradually increased from the delay cell of a front end of the delay line to the delay cell of a rear end of the delay line.

19. (New) A delay-locked loop for receiving an external clock signal and synchronizing a phase of a feedback clock signal with a phase of the external clock signal, the delay-locked loop comprising:

a phase detector for comparing the phase of the external clock signal with the phase of the feedback clock signal and outputting a phase difference as an error control signal;

a delay line, comprising a plurality of delay blocks, each delay block comprising a plurality of delay cells having the same unit time delay, wherein the unit time delay of delay cells from different delay blocks are different, the delay line for receiving the external clock signal, controlling the phase of the external clock signal to obtain an output clock signal and outputting the output clock signal, wherein the number of delay cells in operation is adjusted in response to a shift signal, wherein each delay cell is a differential amplifier having a resistor connected to a power supply voltage, wherein the resistors of the delay cells from different delay blocks have different resistances and the resistors of the delay cells from the same delay block have the same resistance, to vary the unit time delay; and

a filter unit for generating the shift signal for selecting the number of delay cells in operation in the delay line, in response to the error control signal.